design ideas

Edited by Bill Travis and Anne Watson Swager

Low-power PWM circuit is simple, inexpensive

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A COMMON TECHNIQUE for implementing PWM involves comparing a triangular waveform of fixed amplitude and frequency with a variable dc voltage level. Although this approach results in a PWM signal of precise frequency and with duty cycle variable from 0 to 100%, the need for a reference triangle waveform and a suitable fast comparator can be prohibitively expensive in low-cost applications. Furthermore, if an application requires a high-frequency PWM signal, the power consumption may be unacceptable in power-sensitive applications, such as high-efficiency, low-power switch-mode regulators.

The circuit in **Figure 1** is a relatively simple alternative to the triangle/comparator approach. Although the frequency of the output waveform is not stable and varies with input voltage, the circuit is inexpensive, requires only a handful of readily available parts, and exhibits a linear relationship between input voltage and output duty cycle. The circuit lends itself to applications that enclose a simple PWM section within a feedback loop. Also, the excellent dynamics—the duty cycle responds to an input step change within one cycle of the output waveform—make the circuit ideally suited to switch-mode-regulator applications.

In the circuit, the dc input voltage, V_I, varies the duty cycle of the rectangular signal at the output of Schmitt inverter, IC_{1A}. Q_1 and Q_2 function as switched-current sources. These sources charge and discharge timing capacitor C_1 at a rate that their base voltages and, hence, the voltage at the junction of R_2 and R_3 determine. When the output of IC_{1A} is high, C_1 charges through R_6 and Q_1 (Q_2 is cut off) with a charge current set by R_6 and the emitter voltage of Q_1. Similarly, when the output of IC_{1A} is low, C_1 discharges via Q_2 and R_6 (Q_1 is cut off) with a discharge current set by R_6 and the emitter potential of Q_2. Adjusting the input voltage changes the emitter potentials and thus varies the charge and discharge currents so that the duty cycle of the output waveform varies in direct linear proportion to V_I.

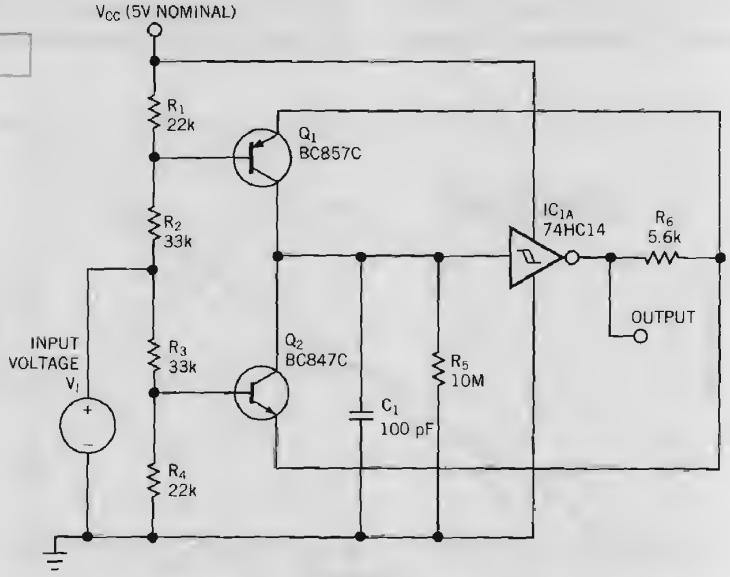
Figure 2 shows the relationship between V_C, which is the voltage on C_1, and the output waveform. V_{TU} and V_{TL} are the upper and lower thresholds of the Schmitt inverter, V_H is the Schmitt trigger's hysteresis, and V_{OH} and V_{OL} are the high and low output levels, respectively, of the inverter.

If you assume that $V_{OH}=V_{CC}$ and $V_{OL}=0V$ and taking the base-emitter voltages of Q_1 and Q_2 to be roughly equal and denoted by V_{BE}, you can derive the following first-order expressions for T_1 and T_2, where $K_1=R_2/(R_2+R_3)$, and $K_2=R_4/(R_3+R_4)$:

$$T_1 = \frac{C_1 \bullet R_6 \bullet V_H}{V_{CC}(1-K_1)+V_I(K_1-1)-V_{BE}},$$

and

Figure 1



In this PWM circuit, adjusting the input voltage, V_I, changes the emitter potentials of Q_1 and Q_2 and thus varies the charge and discharge currents of C_1 so that the duty cycle of the output varies in direct linear proportion to V_I.

$$T_2 = \frac{C_1 \bullet R_6 \bullet V_H}{K_2 \bullet V_I - V_{BE}}.$$

Defining the output duty cycle as equal to $100\% \times T_1/(T_1+T_2)$, you can combine the expression for T_1 and T_2 to yield

$$\text{DUTYCYCLE} = \frac{K_2 \bullet V_I \bullet - V_{BE}}{V_{CC}(1-K_1)+V_I(K_1+K_2-1)-2V_{BE}} \times 100\%.$$

If the R_1-to-R_4 divider network is symmetrical, or $R_1=R_4$ and $R_2=R_3$, this expression simplifies to

$$\text{DUTYCYCLE} = \frac{K_2 \bullet V_I - V_{BE}}{V_{CC}(1-K_1)-2V_{BE}} \times 100\%.$$

Taking the values for R_1 to R_4 in **Figure 1**, the equation reduces to

$$\text{DUTYCYCLE} = \frac{0.4\,V_I - V_{BE}}{0.4\,V_{CC} - 2V_{BE}} \times 100\%.$$

This expression shows that the duty cycle is directly proportional to the input voltage and that V_I must be greater than $V_{BE}/0.4$ for the circuit to work. If $V_{BE}=0.6$V, this equation suggests that V_I must be at least 1.5V, although, in breadboard tests, the circuit produced low duty cycles with V_I as low as 1V.

You select C_1 and R_6 according to the required operating-frequency range. **Figure 3** illustrates the results of breadboard tests with $R_6=5.6$ kΩ and $C_1=100$ pF. The circuit exhibits linear performance with V_I at approximately 1.2 to 3.6V with a corresponding duty-cycle range of approximately 2 to 95%. This **figure** also shows that the output frequency varies by as much as 15 to 1 over this range; the output frequency peaks when V_I is approximately equal to $V_{CC}/2$.

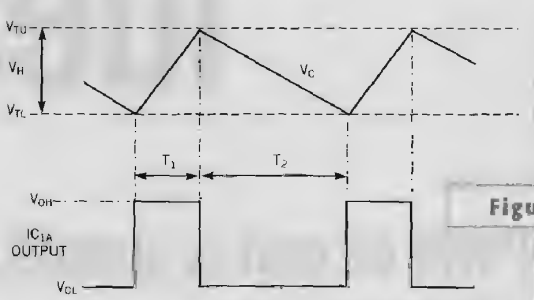


Figure 2

The changing voltage, V_C, across C_1 and the hysteresis, V_H, of IC_{1A} determine the duty cycle, $T_1/(T_1+T_2)$, of the output waveform. V_{TU} and V_{TL} are IC_{1A}'s upper and lower thresholds, respectively.

You need to observe a few caveats when selecting R_1 to R_4 and IC_{1A}. To ensure that the duty cycle is variable from near zero to near 100%, the charge and discharge currents through Q_1 and Q_2 must be able to approach zero. You can meet this requirement simply by ensuring that V_{E1}, or Q_1's emitter potential, can approach V_{CC} and that V_{E2}, or Q_2's emitter potential, can approach ground.

You can make V_{E1} approach V_{CC} when V_I is a maximum by the suitable selection of R_1 and R_2, provided that you choose R_3 and R_4 so that V_{E2} can go a few hundred millivolts below the minimum lower threshold voltage, V_{TL} (minimum), of IC_{1A} when V_I is a maximum. This feature is necessary to ensure that Q_2 does not saturate when V_C approaches V_{TL} (minimum) as C_1 discharges.

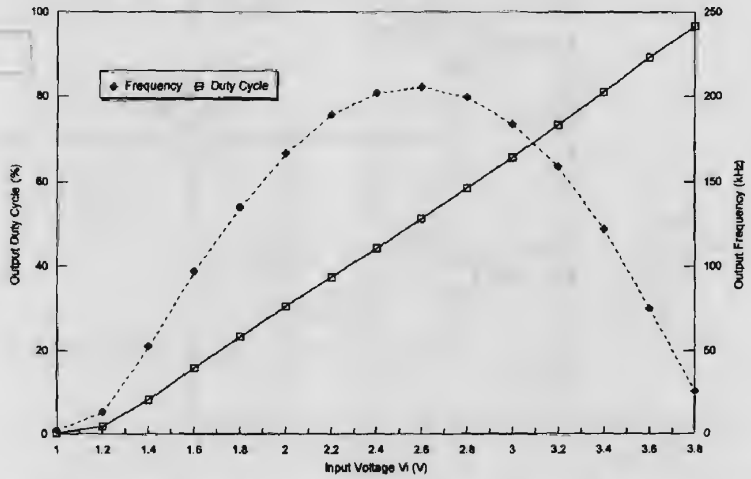
Similarly, by suitably selecting R_3 and R_4, you can make V_{E2} approach zero when V_I is a minimum, provided that you choose R_1 and R_2 so that V_{E1} can go a few hundred millivolts above the maximum upper threshold voltage, V_{TU} (maximum), of IC_{1A} when V_I is a minimum. This feature is necessary to ensure that Q_1 does not saturate when V_C approaches V_{TU} (maximum) as C_1 charges.

The values $R_1=R_4=22$ kΩ and $R_2=R_3=33$kΩ meet these requirements and provide an optimum range for V_I. These values should provide reliable operation for $V_{CC}=5\text{V}\pm5\%$ and IC_{1A} and IC_{1A} = 74HC14, but you may need to recalculate the values if you use a different supply voltage or a different inverter.

Two possible devices to use for IC_{1A} are the 74HC14 and the 4093. The 74HC14 is preferable because the minimum to maximum variation in its hysteresis voltage is only about 3.3 to 1, whereas the variation in V_H for the 4093 is approximately 6.7 to 1. However, the 4093 allows operation at supply voltages greater than 5V, but take care to avoid base-emitter breakdown of Q_1 and Q_2 at higher supply voltages.

Power consumption is low. For example, with $C_1=100$ pF, the maximum current draw is 570 μA at the point of maximum frequency, which is approximately 200 kHz. The maximum practical operating frequency is limited to around 500 kHz ($C_1=10$ pF, $R_6=5.6$kΩ), where the relationship between V_I and the duty cycle starts to become noticeably nonlinear. (DI #2461)

Figure 3



Although the frequency of the output waveform varies with the input voltage, the PWM circuit exhibits a linear relationship between input voltage and output duty cycle.

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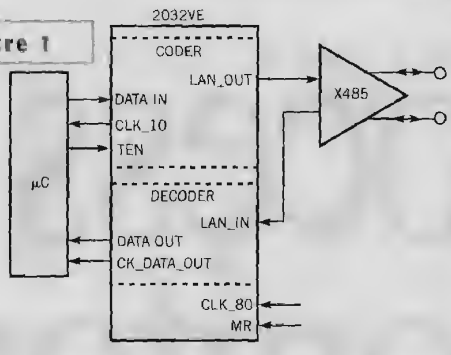
Manchester co-decoder fits into 32-macrocell PLD

Antonio Di Rocco, Siemens ICN Spa, L'Aquila, Italy

Figure 1



A 32-macrocell PLD implements a complete Manchester co-decoder at a 10-MHz bit-speed rate.

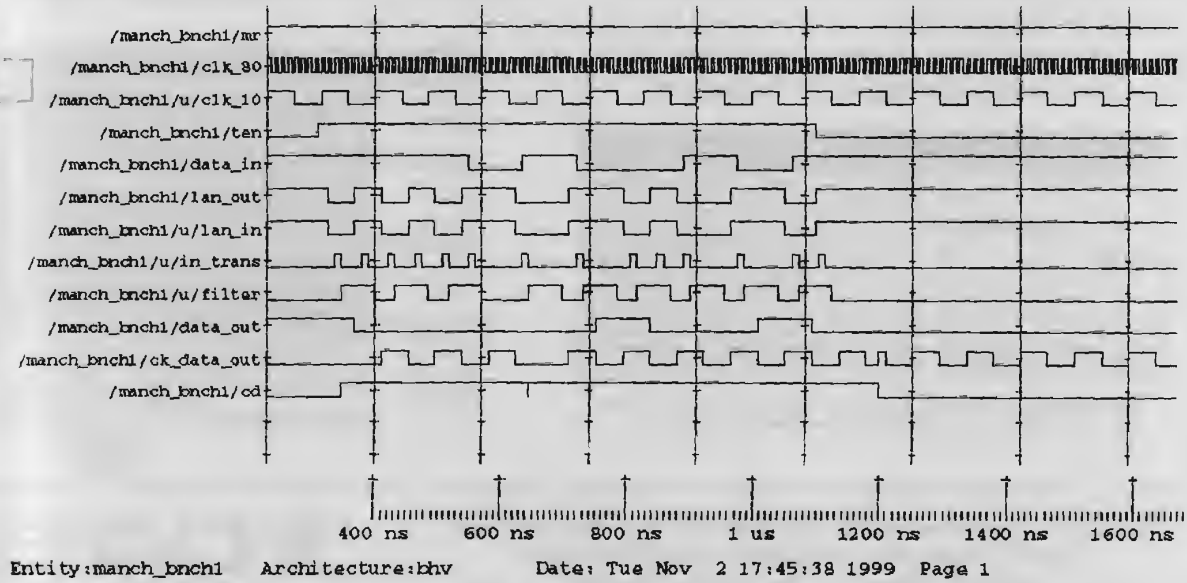
MANCHESTER ENCODING is common, and this scheme erases the dc-spectrum component present in an NRZ signal in baseband transmissions. An important application is in Ethernet-interface adapters, in which several kinds of media-attachment units interface with OSI layers. Many commercial transceivers work on all physical layers of the IEEE 802.3 standard. **Figure 1** and the corresponding source code realize a customized version of the 10BaseT standard in which the physical layer is a coupled stripline in a backplane. **Figure 1** shows the simple schematic of the LAN controller.

With an 80-MHz external clock, the 32-macrocell PLD implements a complete Manchester co-decoder at a 10-MHz bit-speed rate. You can download the VHDL source code from *EDN*'s Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2462.

The Manchester coder comprises an XOR gate between the transmitted data from the µC data_in) and the internal 10-MHz clock. Both the data_in and coded output lan_out signals are synchronous with the 10- and 80-MHz clocks, respectively. Asserting a high at the "10" input enables the coder.

The decoder's operation is more complicated than that of the encoder. A behavioral simulation (**Figure 2**) shows the internal signals that are involved in the decoding process. Note that the spike on the "cd" signal is not a true spike; it appears only in the behavioral simulation and disappears in postlayout simulation. The signal "in_trans" is a short trigger pulse that occurs at every positive and negative "lan_in" transaction. These pulses trigger a filter maker that generates an impulse signal called filter, and each pulse of this filter signal lasts 75% of the bit interval. The end of each filter pulse marks the start of a pulse of a 10-MHz recovered clock. The design generates decoded data by sampling the data stream with the rising edge of the recovered clock. After a bit violation, or when "data_in" remains a one or a zero for more than 100 nsec, the system deasserts the carrier-detect signal, "cd." Many µC families require that five or six recovered clock pulses are present after the system deasserts the carrier-detect signal. To conserve space in the PLD, this design roughly multiplexes the recovered clock and the 10-MHz system clock. (The 68360 µP tolerates one pulse with no aspect of duty cycle.) The carrier-detect signal is the multiplexer controller. The 80-MHz clock has no stability requirements, and the system tolerates jitter on 10-MHz Manchester-coded signals. (DI #2462)

Figure 2



A behavioral simulation of the decoder's operation shows the internal signals involved in decoding.

Input-protection scheme tops other approaches

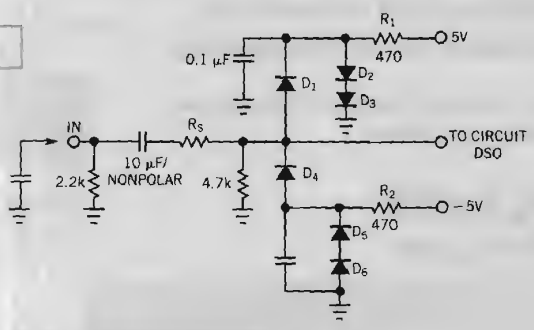
Kannan Natarajan, Mediatronix Private Limited, Kerala, India

You typically accomplish overvoltage or surge protection at circuit inputs by connecting diodes to the supply rails, connecting zener diodes to ground, or connecting transzorbs to ground. Unfortunately, for high-energy surges at the inputs, connecting diodes to the supply rails results in surges in supply lines and affects other components because of the inductance of supply rails, regulator shutdown, and so on. Zener diodes have limited surge capability, and transzorbs have large capacitance and are therefore suited only for low-bandwidth applications.

The circuit in **Figure 1** has many advantages over these approaches: wide bandwidth and low capacitance; high surge-energy handling because the diodes can carry 50A peak; 1A continuous current; and fast response. Also, the circuit doesn't affect the supply rails and is suitable for protecting multiple I/O lines because the lines can share the bias voltage. You can further improve the response time by using faster diodes; a ground plane; low-inductance, short connections; and close, high-frequency decoupling.

The circuit reverse-biases D_1 and D_4 to bias voltages of ±1.2V, respectively. R_1 and R_2 bias two pairs of diodes, D_2/D_3 and D_5/D_6, respectively, to generate the ±1.2V. R_1 and R_2 prevent input surges from reaching the supply rails. The surge shunt path consists of D_1, D_2, and D_3 to ground or D_4, D_5, and D_6 to ground, depending on the surge's polarity. Because of the ±12V bias-voltage settings, the circuit works with maximum input signals of ±1V. Above this level, D_1 and D_4 start to leak and distort the signal. The circuit was tested using a 100-µF/50V test capacitor charged to 30V and then discharged to the input. A DSO captured the results (**Figure 2**). In **Figure 2a**, with R_S= 100Ω, the peak is approximately 3.5V, and settling to around 2V occurs within 15 nsec. **Figure 2b** shows the same response as **Figure 2a** but with a horizontal scale of 1 msec/div. **Figure 2c** is also the response under the same conditions but shows the long-term response and the coupling-capacitor recovery. If you let R_S=0, the peak rises to 10V and settles within 500 nsec. Thus, some small resistance, such as 100Ω, is necessary for R_S. (DI #2463)

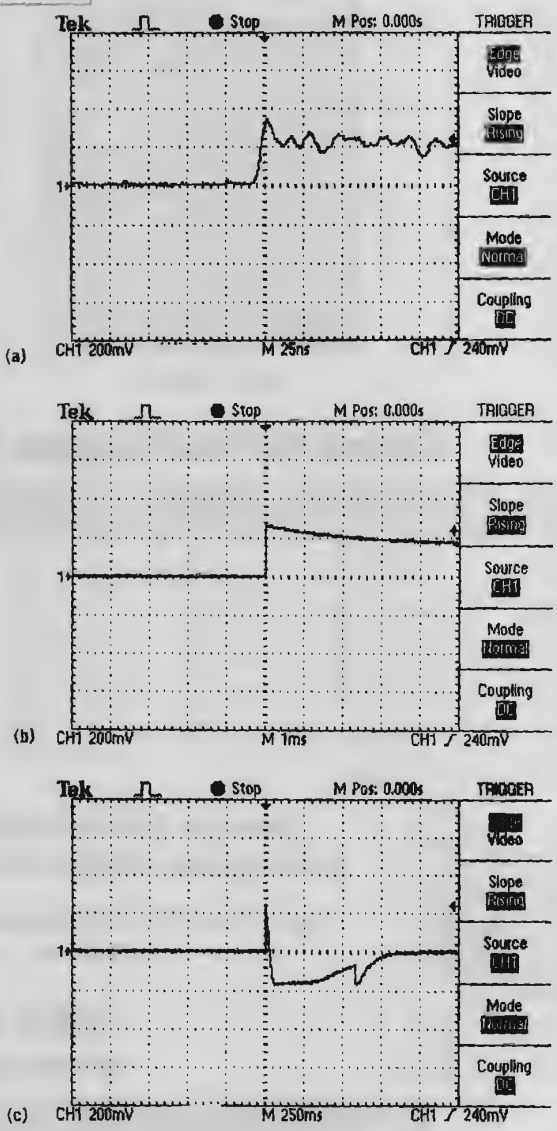
Figure 1



NOTES: ALL DIODES=1N4935 FAST-RECOVERY TYPE.

Two surge shunt paths, consisting of D_1, D_2, and D_3 to ground or D_4, D_5, and D_6 to ground, provide overvoltage protection.

Figure 2



Tests with a 30V charged capacitor at the input show the circuit's response with a horizontal scale of 25 nsec/div (a) and 1 msec/div (b). The long-term response shows the recovery of the coupling capacitor (c).

Level-shifting nixes need for dual power supply

Ron Olmstead, Westcor, Sunnyvale, CA

The AD736 true-rms-to-dc converter is useful for many applications that require precise calculation of the rms value of a waveform. This converter can determine the true rms value, the average rectified value, or the absolute value of a myriad input waveforms. Basically, all applications require both a positive and a negative power supply. According to the data sheet, you can use the device with a single supply by ac-coupling the input signal and biasing the common pin above ground. However, the ability to process only ac signals is a major performance limitation. You can lift this limitation by using a level-shifting approach (**Figure 1**). This approach requires more circuitry, but it removes the ac-only input-waveform restriction.

The circuit consists of three sections. The first is a differential amplifier that adds the level-shifting offset, V_{REF}, to the input waveform. This amplifier's primary function is to level-shift the waveform, but it can also provide gain and filtering if necessary. The output of the op amp needs to swing to the value of V_{REF} minus the peak negative swing of the input waveform times the gain of the op amp ($V_{REF}-(A\cdot V_{IN})$) and to the value of V_{REF} plus the peak positive swing of the input voltage times the gain of the op amp ($V_{REF}+(A\cdot V_{IN})$). By adjusting the value of V_{REF} and the gain of the op amp, you can eliminate the need for an expensive rail-to-rail op amp and can then use any single-supply op amp. All three sections use the same level-shifting offset, V_{REF}.

The second section is the rms-to-dc-converter stage. The output of this stage is the dc (rms) value of the input waveform plus the offset value (V_{REF}). The input voltage divider reduces the amplitude of the input waveform. For successful rms-to-dc conversion, the circuit must keep the voltage going into the AD736 within the specified range, which is 1V rms for a V_{CC} of ±5 to ± 16V. If amplitude reduction is unnecessary, you can eliminate these resistors and simply ground Pin 1 of the AD736. The offset voltage needs to connect to the AD736 (**Figure 1**). This connection provides a reference for the circuit that is above ground. The AD736 cannot provide accurate calculations for inputs that go below or even equal the converter's negative rail, $-V_S$. V_{REF} should be greater than the peak negative swing of the input waveform. V_{CC} should be greater than V_{REF} plus the peak positive swing of the input voltage.

The third section of the circuit is a level-shifting circuit, which subtracts V_{REF} from the output of the AD736. The last-stage differential amplifier can provide any necessary gain, and you can use this gain to eliminate the need for a rail-to-rail op amp.

The application of the circuit in **Figure 1** is to measure the current draw of a power supply and detect overcurrent conditions. For this application, only a positive power supply was available. The input op amp raises the amplitude of the input signal and filters out any noise greater than 5 kHz. The power-supply input is a three-phase 60-Hz signal, so the ripple frequency is 360 Hz. By providing gain in this first stage and a 5V level shift, any single-supply op amp is suitable. Also, a rail-to-rail op amp is unnecessary. The circuit divides down the output of the first stage to be sure not to exceed the input voltage range of the AD736. The output amplifier provides gain to the dc signal and level-shifts the signal back to a ground-referenced signal. Again, the gain of this op amp produces a signal with an amplitude suitable for use with any single-supply op amp. (DI #2466)

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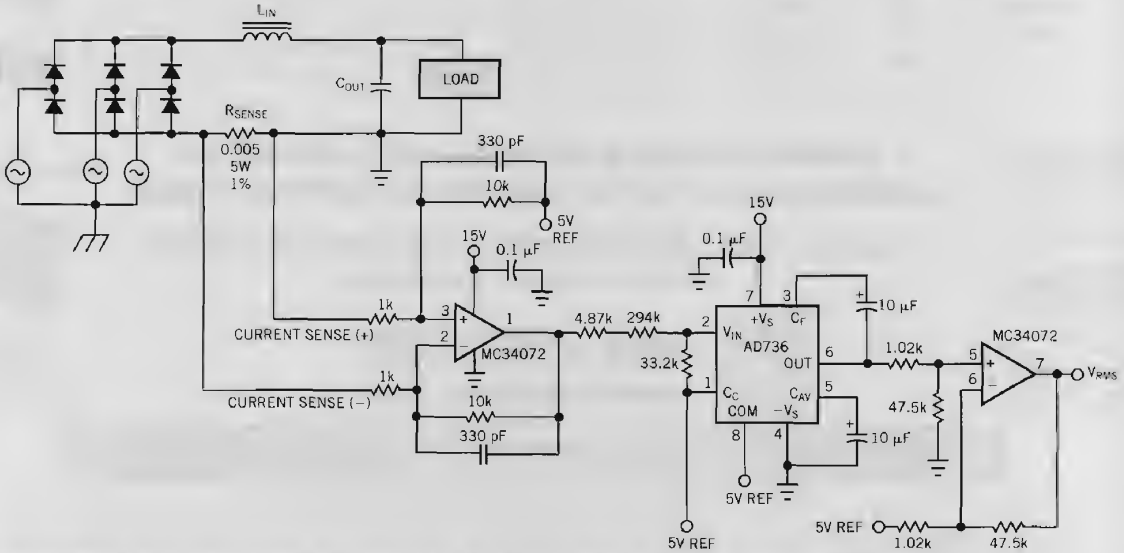
Figure 1



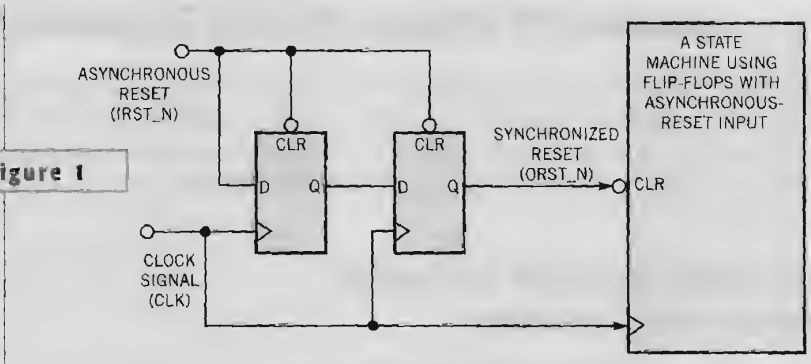
Level-shifting the input to an rms-to-dc converter allows you to use the converter with only positive supply voltages.

Synchronize asynchronous reset

Willy Tjanaka, Philips Semiconductors, Sunnyvale, CA

SYNCHRONOUS RESET and asynchronous RESET are both common reset mechanisms for state machines, and the reset circuit in **Figure 1** combines the advantages of each. Synchronous reset has the advantage of synchronization between clock and reset signals, which prevents race conditions from occurring between the clock and the reset signal. However, synchronous reset does not allow a state machine to operate down to a dc clock because reset does not occur until a clock event occurs. In the meantime, uninitialized I/O ports can experience severe signal contention.

Figure 1



A simple circuit combines the advantages of asynchronous and synchronous resets.

Asynchronous reset has the advantage of allowing state machines to operate down to dc clock. This operation is possible because asynchronous reset immediately initializes the state machine when a reset signal occurs independently of the clock. Unfortunately, asynchronous reset may cause a race condition between the reset signal and the clock. Race conditions can cause problems, including metastability or wrong-state initialization.

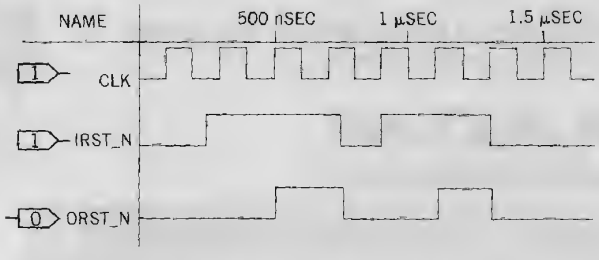
The reset circuit in **Figure 1** asserts the reset signal immediately after detecting the asynchronous reset signal. However, the circuit also synchronizes the reset release with the clock. The circuit uses this synchronized asynchronous-reset signal to drive a state machine that uses flip-flops and the asynchronous-reset input.

LISTING 1—VERILOG DESCRIPTION OF THE SYNCHRONIZED ASYNCHRONOUS-RESET CIRCUIT

```
module reset (clk, irst_n, orst_n);
// Willy Tjanaka
// Rev. 1.0, 17 October 1999

input  clk, irst_n;
output orst_n;
reg    orst_n, mrst_n;

always @ (posedge clk or negedge irst_n)
begin
  if (!irst_n)
  begin
    mrst_n <= 1'b0;
    orst_n <= 1'b0;
  end

  else
  begin
    mrst_n <= irst_n;
    orst_n <= mrst_n;
  end
end

endmodule
```

The reset circuit consists of two back-to-back D flip-flops that synchronize the asynchronous reset signal. In addition, the asynchronous reset causes the D flip-flop outputs to immediately go low. **Figure 1** also shows the corresponding signal names for the Verilog description of the circuit (**Listing 1**), which you can immediately incorporate into a design or simulation. **Figure 2** shows the simulation waveform from the Verilog code in **Listing 1** using Altera Max+PlusII. Observe that the circuit immediately asserts the output-reset signal (orst_n) when the system asserts the input reset signal, irst_n. Also notice that the reset release is synchronous with the clock within two cycles. (DI #2465)

Figure 2



The simulation waveform shows that the circuit asserts the output reset signal, orst_n, immediately after the system asserts the asynchronous input signal, irst_n, and shows that the reset release is synchronous with the clock signal within two cycles.

Circuit resolves 0.1-fF change from 100 pF

Derek Redmayne, Linear Technology Corp, Milpitas, CA

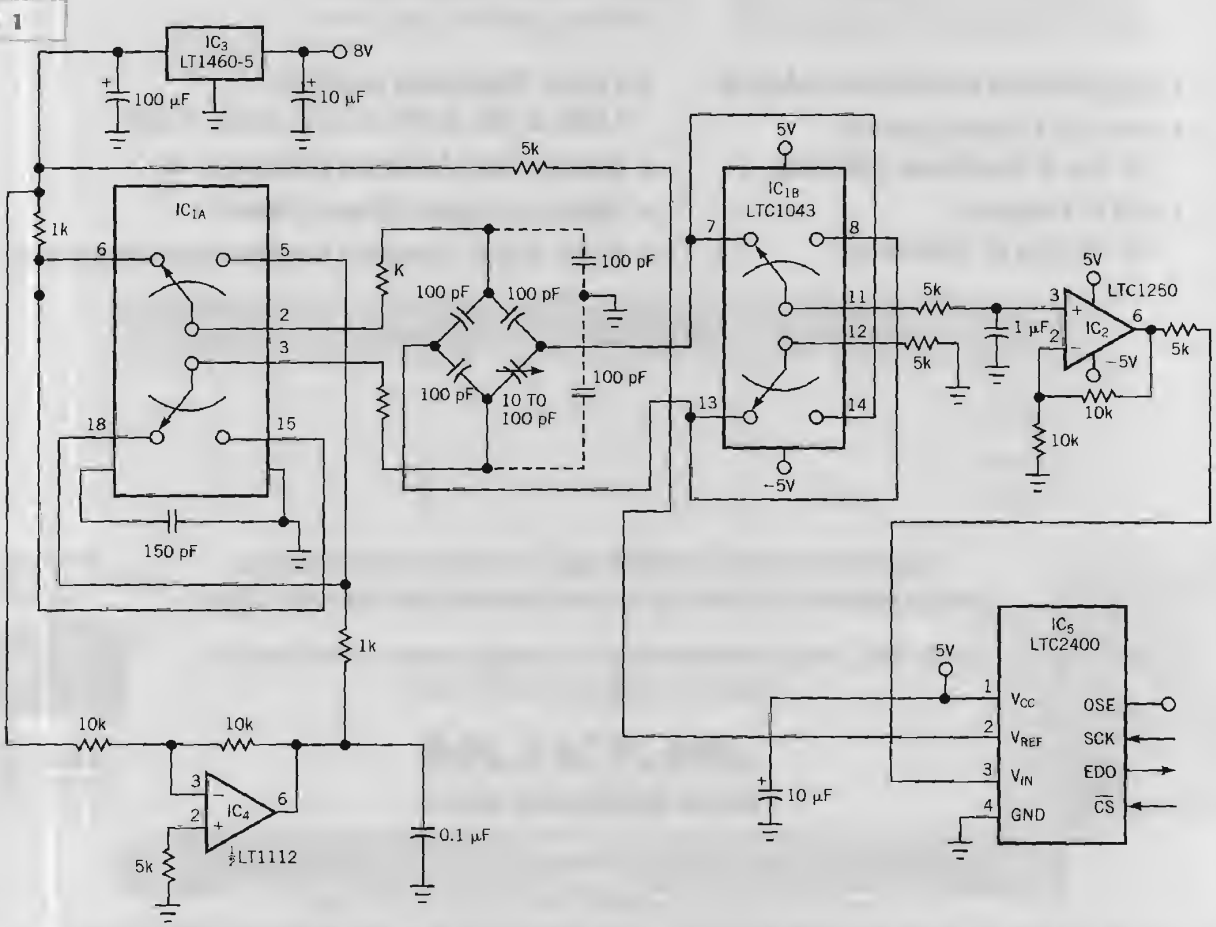
THE CIRCUIT IN **Figure 1** can resolve 0.1-fF changes in a 100-pF bridge element and can accommodate large-scale changes in the bridge without adjustment. You can use changes in capacitance to measure applied pressure, rotation, torque, liquid level, the water content of toast, and a host of other things. Many variants of the circuit are possible.

IC_1, an analog switch, provides both bridge excitation and synchronous rectification. A chopper-stabilized amplifier, IC_2, which the circuit configures for a gain of 2, buffers and amplifies the output of the synchronous rectifier, IC_{1B}. No amplification occurs before the rectification stage. IC_1's internal oscillator and an external capacitor determine the frequency of the square-wave excitation signal—in this case, 20 kHz—that the circuit delivers to the bridge via IC_{1A}.

If, as in this case, the excitation waveform is essentially a square wave, the system is not oversensitive to oscillator frequency and thus not oversensitive to the supply voltage. This circuit reduces the slew rates of the excitation to reduce EMI and to prevent transient load changes from disturbing the reference and buffer, IC_3 and IC_4, respectively. Further significant reductions in the slew rate cause the frequency of commutation in IC_1 to affect the output. A delta-sigma ADC, IC_5, resolves the output of amplifier IC_2 to approximately 1 ppm.

You can use a capacitance change of this magnitude to measure subtle changes in dielectric constant, such as

Figure 1



Using an analog switch, IC_1; a chopper-stabilized amplifier, IC_2; a reference, IC_3; a buffer, IC_4; and a delta-sigma ADC, IC_5, this circuit can resolve 0.1-fF changes in a 100-pF bridge element.

those that may occur in oil due to contamination. For example, if you create a capacitor using 5×5-in. plates that are ¼ in. apart, the dielectric constant, K, of the media between the plates could be resolvable over the range of 1 to 4.5 (22.48 to 101.2 pF). A change in K of as little as 0.000004 would be measurable. The rigidity and separation between these plates would have to be constant and stable because movement of as little as 0.3 µm would produce the same 0.1-fF change. The use of low-thermal-coefficient materials would be necessary to maintain this separation, but this measurement is practical with good mechanical design.

Other capacitor geometries are possible, of course. For example, the plates of the capacitor could be coplanar interleaved fingers etched onto an insulator, and the unknown dielectric could either touch the surface or be distanced with an insulator. Also, many configurations of bridges are possible. For example, you could devise bridges to compare two substances. You could also construct bridges to deflect the field toward the plates of one capacitor or another, depending on the K of some substance running through channels—for example, to compare the dielectric constant of two liquids. Assuming good sensor design, E-field (ac) measurements can be comparatively free of the effects, including drift, hysteresis, creep, nonlinearities, thermocouple effects, self-heating, leakage, and electromigration that compromise dc measurements.

The circuit in **Figure 1** is usable, but you can improve the circuit's long-term drift and temperature stability by deriving a timing signal from a quartz oscillator. Note that resolving small capacitance changes requires diligent attention to parasitics. If a single variable capacitor, as in this example, sits remotely from the other bridge elements, it is recommended that you use shielded cable with the shield driven from either the other bridge arm or even a third arm (see the dashed line in **Figure 1**). If this situation occurs, you should route the lower end of the bridge separately to the external capacitor. If you plan to bundle these cables, you should use the upper arm of the excitation to shield the excitation to the lower end of the unknown capacitor. This cable capacitance loads and hence attenuates the bridge drive, and you should perhaps use a separate synchronized analog switch to sense these loads to provide a reference signal for ratiometric operation.

Alternatively, you can ground the shield if the bridge is symmetrical about the midpoint. If the bridge is asymmetrical, the inputs to IC_1 see a substantial ac component. You can potentially drive an asymmetrical bridge with a transformer and ground the midpoint of the third arm to reduce the common mode seen in the taps. (DI #2464)

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